UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/633,087	08/04/2000	Derrick R. Meyer	(TT3327)	1102

7590 10/20/2006

Diana M Sangalli
Fletcher Yoder & Van Someren
P O Box 692289
Houston, TX 77269-2289

EXAMINER	
BURGESS, BARBARA N	
ART UNIT	PAPER NUMBER
2157	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/633,087	MEYER ET AL.	
	Examiner	Art Unit	
	Barbara N. Burgess	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12,14-24 and 27-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12,14-24 and 27-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7-19-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Amendment filed July 6, 2004. Claims 6, 13, 25-26 have been cancelled as requested by Applicant. Claims 1-5, 7-12, 14-24, 27-33 are presented for further examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7-12, 14-21, 23, 27-33 are rejected under 35 U.S.C. 102(b) as being unpatentable over Higuchi et al. (hereinafter "Higuchi", 5,774,731) in view of Chan (US Patent 6,920,454 B1).

As per claims 1, 15, Higuchi discloses in a multiprocessing computer system comprising a plurality of processing nodes interconnected through an interconnect structure, wherein the plurality of processing nodes includes a first processing node, a second processing node, and a third processing node, a method for lock request arbitration comprising:

- The first processing node transmitting a lock request to the second processing node (column 5, lines 53-58, column 6, lines 21-25, column 7, lines 34-38, column 8, lines 21-27, 44-46, 57-60, column 20, lines 17-22, 42-48, column 21, lines 15-18);

- The second processing node determining whether the lock request is ready for service (column 2, lines 65-67, column 3, lines 1-2, 6-10, column 6, lines 25-27, column 7, lines 36-38, column 8, lines 8-10, 21-27, 40-41, column 13, lines 1-3, column 20, lines 46-47);
- The second processing node issuing a broadcast message to the first and the third processing nodes in response to determining that the lock request is ready for service (column 8, lines 21-27, column 10, lines 35-50, column 20, lines 19-22, 45-49, 55-58);

Higuchi does not explicitly disclose:

- The first processing node sending a first probe response to the second processing node in response to the broadcast message;
- The third node sending a second probed response to the second processing node in response to the broadcast message.

However, in an analogous art, Chan discloses nodes receiving a broadcast message from a first master node. The nodes then re-map hash values and send an acknowledgement to the first master node (column 6, lines 25-33, column 20, lines 18-21, 33-40, 45-49).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Chan's second processing node issuing a broadcast message to first and third processing nodes and these node in response sending probing responses to the second processing node in Higuchi's

system to acknowledge that the broadcast message had been received from the master node.

As per claims 2, 16, Higuchi discloses wherein determining whether the lock request is ready for service comprises:

- The second processing node placing the lock request in a queue (column 30, lines 20-30, 44-46, 63-67, column 31, lines 1-45, column 36, lines 53-58);
- The second processing node monitoring the queue to determine whether the lock request is ready for service (column 30, lines 20-30, 44-46, 63-67, column 31, lines 1-45, column 36, lines 53-58).

As per claim 3, Higuchi further discloses wherein monitoring the queue comprises:

- Sequentially processing each preceding lock request in the queue (column 30, lines 20-30, 44-46, 63-67, column 31, lines 1-45, column 36, lines 53-58).

As per claim 4, Higuchi discloses wherein the broadcast message informs the third processing node of servicing of the lock request (column 8, lines 21-27, column 10, lines 35-50, column 20, lines 19-22, 45-49, 55-58).

As per claims 5, 17, Higuchi discloses wherein the broadcast message includes a lock bit to inform the third processing node of the servicing of the lock request (column 11, lines 17-40, column 13, lines 28-40, column 14, lines 25-34, column 19, lines 25-40).

As per claim 7, Higuchi discloses wherein the third processing node sends the second probe response when the third processing node ceases issuance of new requests (column 30, lines 20-30, 44-46, 63-67, column 31, lines 1-45, column 36, lines 53-58).

As per claim 8, Higuchi discloses the second processing node informing the first processing node of availability of lock ownership upon receiving the first and the second probe response messages (column 3, lines 12-17, column 8, lines 38-41, column 23, lines 16-20).

As per claim 9, Higuchi discloses wherein the second processing node informing the first processing node comprises:

- The second processing node transmitting a target done message to the first processing node to indicate the lock ownership (column 2, lines 65-67, column 3, lines 1-2, 6-10, column 6, lines 25-27, column 7, lines 36-38, column 8, lines 8-10, 21-27, 40-41, column 13, lines 1-3, column 20, lines 46-47).

As per claim 10, Higuchi discloses in a multiprocessing computer system comprising a plurality of processing nodes interconnected through an interconnect structure, wherein the plurality of processing nodes includes a first processing node, a second

processing node, and a third processing node, a method for lock request arbitration comprising:

- The first processing node transmitting a lock release request to the second processing node (column 17, lines 10-36, column 23, lines 55-57);
- The second processing node issuing a broadcast message to the first and the third processing nodes in response to the lock release request (column 17, lines 10-36, column 23, lines 55-57).

Higuchi does not explicitly disclose:

- Each of the first and third processing nodes sending a first corresponding probe response message to the second processing node in response to the broadcast message.

However, in an analogous art, Chan discloses nodes receiving a broadcast message from a first master node. The nodes then re-map hash values and send an acknowledgement to the first master node (column 6, lines 25-33, column 20, lines 18-21, 33-40, 45-49).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Chan's second processing node issuing a broadcast message to first and third processing nodes and these node in response sending probing responses to the second processing node in Higuchi's system to acknowledge that the broadcast message had been received from the master node.

As per claim 11, Higuchi discloses wherein the broadcast message informs the third processing node of completion of lock operations within the multiprocessing computer system (column 17, lines 10-36, column 23, lines 55-57).

As per claim 12, Higuchi discloses wherein the broadcast message includes a lock bit to inform the third processing node of the completion of the lock operations (column 11, lines 17-40, column 13, lines 28-40, column 14, lines 25-34, column 17, lines 10-36, column 19, lines 25-40, column 23, lines 55-57).

As per claim 14, Higuchi discloses the second processing node transmitting a corresponding target done message to the first processing node upon receiving the first corresponding target done messages from the first and the third processing nodes (column 17, lines 10-36, column 23, lines 55-57).

As per claim 18, Higuchi discloses wherein the interconnect structure includes a plurality of dual-unidirectional links (column 5, lines 25-45).

As per claim 19, Higuchi discloses wherein each dual-unidirectional link in the plurality of dual-unidirectional links interconnects a respective pair of processing nodes from the plurality of processing nodes (column 5, lines 25-45).

As per claim 20, Higuchi discloses wherein each dual-unidirectional link in the plurality of dual-unidirectional links performs packet zed information transfer (column 5, lines 25-45).

As per claim 21, Higuchi discloses wherein each of the plurality of processing nodes includes:

- A plurality of circuit elements comprising:

  A processor core (column 7, lines 14-35);

  A cache memory (column 7, lines 14-35);

  A memory controller (column 7, lines 14-35);

  A plurality of interface ports, wherein each of the plurality of circuit elements is coupled to at least one of the plurality of interface ports (column 7, lines 14-35, column 9, lines 12-30).

As per claim 23, Higuchi discloses wherein at least one of the plurality of interface ports in the each of the plurality of processing nodes is connected to a corresponding one of the plurality of dual-unidirectional links (column 7, lines 14-35, column 9, lines 12-30).

As per claim 27, Higuchi discloses wherein the second processing node is further configured to cease issuance of new requests and to transmit the corresponding first

probe response message upon the cessation of the issuance (column 30, lines 20-30, 44-46, 63-67, column 31, lines 1-45, column 36, lines 53-58).

As per claim 28, Higuchi discloses wherein the third processing node is configured to transmit a first target done message to the first processing node after receiving the corresponding probe response messages from the first and the second processing nodes (column 17, lines 10-36, column 23, lines 55-57).

As per claim 29, Higuchi discloses wherein the first processing node is configured to commence the execution of the lock operation after receiving the first target done message, and wherein the first processing node is further configured to transmit a lock release request to the third processing node after completion of the execution of the lock operation (column 17, lines 10-36, column 23, lines 55-57).

As per claim 30, Higuchi discloses wherein the third processing node is configured to transmit a second broadcast message to the first and the second processing nodes in response to receiving the lock release request (column 17, lines 10-36, column 23, lines 55-57).

As per claim 31, Higuchi discloses wherein each of the first and the second processing nodes is configured to transmit a corresponding second probe response

message to the third processing node in response to the second broadcast message (column 3, lines 12-17, column 8, lines 38-41, column 23, lines 16-20).

As per claim 32, Higuchi discloses wherein the third processing node is configured to transmit a second target done message to the first processing node in response to receiving the corresponding second probe response messages from the first and the second processing nodes (column 17, lines 10-36, column 23, lines 55-57).

As per claim 33, Higuchi discloses wherein the third processing node is configured to place a pending lock request into service upon transmission of the second target done message, and the pending lock request is generated by one of the plurality of processing nodes and is stored within the third processing node (column 2, lines 65-67, column 3, lines 1-2, 6-10, column 6, lines 25-27, column 7, lines 36-38, column 8, lines 8-10, 21-27, 40-41, column 13, lines 1-3, column 20, lines 46-47).

3. Claims 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi et al. (hereinafter "Higuchi", 5,774,731) in view of Chan (US Patent 6,920,454 B1) and in further view of Shrivastava et al. (hereinafter "Shriva", 6,163,855)

As per claim 22, Higuchi, in view of Chan, does not explicitly disclose wherein the plurality of circuit elements further includes:

- A bus bridge;
- A graphics logic;

- A bus controller ;
- A peripheral device controller.

However, the advantages and use for such circuit elements is well known to one skilled in the relevant art at the time the invention was made as evidenced by Shriva (column 3, lines 12-45).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate these elements in Higuchi in order to receive information about what device has control of the lock.

As per claim 24, Higuchi, in view of Chan, does not explicitly disclose the multiprocessing computer system comprising:

- A plurality of memory buses, wherein each of the plurality of system memories is coupled to a corresponding one of the plurality of system buses.

However, the advantages and use for such memory buses is well known to one skilled in the relevant art at the time the invention was made as evidenced by Shriva (column 3, lines 12-45).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate memory buses in Higuchi in order to receive information about what device has control of the lock.

Response to Arguments

4. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barbara N. Burgess whose telephone number is (571) 272-3996. The examiner can normally be reached on M-F (8:00am-4:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571) 272-4001. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barbara N Burgess
Examiner
Art Unit 2157

October 15, 2006

ABDULLAHI SALAD
PRIMARY EXAMINER